First Laureate
Applied Research

Project Title: Design and analysis of high performance and low power computer architecture based on the nation of Network-on-Chip (NoC)
Researcher: Prof. Nader Bagherzadeh
Country: Iran (Iranian resident in USA)
Field: Computer Engineering
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Abstract:

As the number of cores for a System-on-Chip (SoC) increase to hundreds of units, it will be much harder to use the same old techniques based on the bus central architecture to develop the next generation SoCs. Long wires due to bus central designs result in wire delays that require multiple clock cycles to traverse across the chip. These designs tend to be slow and require power consumption levels that are not acceptable for embedded systems as well as high performance machines. In this work we are investigating the notion of Network-on-Chip (NoC) for the design of future generation SoCs. We have developed efficient new routers for managing packets, devised new mapping and scheduling algorithms for executing tasks on multiple cores, and introduced new modeling approaches for evaluating the behavior of NoC architectures under realistic work load conditions. We also plan to extend our work to 3D NoCs.

Biography:

Nader Bagherzadeh is a professor of computer engineering in the department of electrical engineering and computer science at the University of California, Irvine, where he served as a chair from 1998 to 2003. Prof. Bagherzadeh has been involved in research and development in the areas of: computer architecture, reconfigurable computing, VLSI chip design, network-on-chip, 3D chips, sensor networks, and computer graphics since 1987.

Professor Bagherzadeh has published more than 200 articles in peer-reviewed journals and conferences. He has trained hundreds of students who have assumed key positions in software and computer systems design companies in the past twenty years.